R22

Code No: R22A1261

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, June 2025

Computer Organization & Architecture

(CSE-CS, CSE-AIML, CSE-IOT & B.Tech-AIML)

Roll No										

Time: 3 hours **Max. Marks: 60**

Note: This question paper contains two parts A and B
Part A is compulsory which carries 10 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

***

		PART-A (10 Marks) **(Write all answers of this part at one place)**	**BCLL**	**CO(s)**	**Marks**
1	A	How the characters are represented in computer?	**L2**	**CO-I**	**[1M]**
	B	What is the range of values represented using 8-bits in 2's complement notation?	**L3**	**CO-I**	**[1M]**
	C	What is instruction code?	**L2**	**CO-II**	**[1M]**
	D	A computer system uses 16 registers. How many bits required for referring a register in the instruction code?	**L3**	**CO-II**	**[1M]**
	E	Why do Read only Memories are required in the computer?	**L3**	**CO-III**	**[1M]**
	F	What is Hit Ratio?	**L2**	**CO-III**	**[1M]**
	G	Why an IO Interface is required in IO System?	**L3**	**CO-IV**	**[1M]**
	H	Differentiate between Interrupt and Exceptions.	**L2**	**CO-IV**	**[1M]**
	I	What are the challenges to implement parallel processor architecture?	**L2**	**CO-V**	**[1M]**
	J	How many clock cycles required in pipeline for the given n tasks and k stages?	**L3**	**CO-V**	**[1M]**
		PART-B (50 Marks) **SECTION-I**			
2	A	Explain the following components in computer system i) Central Processing Unit ii) Main Memory	**L2**	**CO-I**	**[5M]**
	B	Explain addition and subtraction of 2's complement data.	**L3**	**CO-I**	**[5M]**
		OR			
3	A	Demonstrate with a neat sketch and example Ripple carry adder circuit.	**L2**	**CO-I**	**[5M]**
	B	Perform the multiplication of +14 and +8 using shift-and add algorithm.	**L3**	**CO-I**	**[5M]**
		SECTION-II			
4	A	What is the use of Register Transfer Language? Explain	**L2**	**CO-II**	**[5M]**

		the various arithmetic micro operations.			
	B	How do addressing mode useful in instruction execution? Explain the following addressing modes. i) Register Indirect Addressing Mode ii) Base Register Addressing Mode	**L2**	**CO-II**	**[5M]**
		OR			
5	A	Write the instruction code format and explain shift instructions.	**L2**	**CO-II**	**[5M]**
	B	What is micro-programmed control? Describe the hardware diagram to implement micro-programmed control.	**L3**	**CO-II**	**[5M]**
		SECTION-III			
6	A	How the Semiconductor Memories are classified? Demonstrate with a diagram typical RAM chip.	**L2**	**CO-III**	**[5M]**
	B	Illustrate with an example how direct mapping is used for mapping cache and main memory.	**L3**	**CO-III**	**[5M]**
		OR			
7	A	Differentiate between Main memories and Cache Memories.	**L2**	**CO-III**	**[5M]**
	B	Describe the various cache replacement policies. Identify the pros and cons in it.	**L2**	**CO-III**	**[5M]**
		SECTION-IV			
8	A	How do internal and external components connected in a system? Differentiate between memory mapped IO and Isolated IO.	**L2**	**CO-IV**	**[5M]**
	B	Illustrate with a neat sketch Interrupt driven mode of IO Transfer.	**L3**	**CO-IV**	**[5M]**
		OR			
9	A	What are the limitations of Programmed Control? Explain how it can be resolved using DMA transfer.	**L3**	**CO-IV**	**[5M]**
	B	What is privileged instruction? Why it is required for interrupt handling? Describe the process of handling interrupt in a system.	**L2**	**CO-IV**	**[5M]**
		SECTION-V			
10	A	What is an arithmetic pipeline? How does it improve the performance of a system? Demonstrate with an example.	**L3**	**CO-V**	**[5M]**
	B	How do snoopy cache controller works in parallel architectures? Describe with an example.	**L3**	**CO-V**	**[5M]**
		OR			
11	A	What are the various hazards on pipeline? How do you overcome the structural hazards in instruction pipeline?	**L3**	**CO-V**	**[5M]**
	B	Identify the various interconnection structures for parallel processors. Illustrate with a neat sketch multi stage switching network structure.	**L3**	**CO-V**	**[5M]**

***